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IMPROVED INTEGRATED CIRCUIT BURN-IN METHODS AND APPARATUS

INVENTORS

David H. Pullen

Richard Kacprowicz

Schwegman, Lundberg, Woessner & Kluth, P.A.
1600 TCF Tower
121 South Eighth Street
Minneapolis, MN 55402
ATTORNEY DOCKET SLWK 884.414US1
Client Ref. No. P10930

Improved Integrated Circuit Burn-In Methods and Apparatus

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Technical Field of the Invention

The present invention relates generally to the field of electronics and, more particularly, to improved methods and apparatus for performing burn-in testing on electronic components such as integrated circuits.

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Background of the Invention

In the field of electronic systems there is an incessant competitive pressure among manufacturers to drive the performance of their equipment up while driving down production costs. This is particularly true regarding the testing of integrated circuits (hereinafter "ICs"). ICs must generally be tested before they are incorporated into an electronic assembly in order to verify that each element on the IC functions properly.

It is well known to perform accelerated life testing on ICs to ensure that the ICs do not prematurely fail when they have been incorporated into higher levels of electronic packaging, such as a computer systems, (e.g., desktop, laptop, hand-held, server, etc.), wireless communications devices (e.g., cellular phones, cordless phones, pagers, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, MP3 (Motion Picture Experts Group, Audio Layer 3) players, etc.), and the like.

A goal of burn-in is to provide infant-mortality screening of ICs for reliability defects. By operating the ICs at increased voltage and/or temperature levels, while stimulating as many transistors on the ICs as possible, ICs that might fail prematurely are identified early and pulled out prior to shipment to customers. It is desirable to keep burn-in time (BITM) to a minimum to reduce production costs.

As high performance ICs are packed with increasing numbers of transistors numbering in the millions, the transistor channel length L_e has been made increasingly

shorter to improve performance. Generally, the shorter the channel length L_e the higher the leakage current I_{SB} . As the leakage current I_{SB} increases, so does the corresponding power requirement, and the attendant heat dissipation. Thus, testing large quantities of ICs can require substantial consumption of electrical power resources, even as such
5 resources become increasingly scarce and costly.

It is desirable to thoroughly test ICs undergoing burn-in testing while at the same time minimizing the cost, time, and complexity of such testing.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present
10 specification, there is a significant need in the art for improved IC burn-in methods and apparatus.

Brief Description of the Drawings

15 FIG. 1 illustrates a block diagram of a system to perform component burn-in testing and binning, in accordance with one embodiment of the invention;

FIG. 2 illustrates an IC comprising devices to implement burn-in testing and binning, in accordance with one embodiment of the invention;

20 FIG. 3 is a simplified view of several electronic components mounted on a burn-in test fixture, in accordance with one embodiment of the invention;

FIG. 4 is a simplified view of burn-in test fixtures in a burn-in oven, in accordance with one embodiment of the invention; and

25 FIGS. 5A and 5B together illustrate a flow diagram of an improved method of testing an IC comprising a plurality of electronic devices, in accordance with one embodiment of the invention;

FIGS. 6A and 6B together illustrate a flow diagram of an improved method of testing a plurality of electronic components, such as ICs, in accordance with one embodiment of the invention; and

30 FIGS. 7A and 7B together illustrate a flow diagram of a method of instructing a processor to perform a method of binning a plurality of ICs, wherein each IC has a

thermal sense circuit and a unique identifier, in accordance with one embodiment of the invention

Detailed Description of Embodiments of the Invention

5 In the following detailed description of embodiments of the invention, reference
is made to the accompanying drawings which form a part hereof, and in which is shown
by way of illustration specific preferred embodiments in which the inventions may be
practiced. These embodiments are described in sufficient detail to enable those skilled in
the art to practice the invention, and it is to be understood that other embodiments may
10 be utilized and that logical, procedural, mechanical, and electrical changes may be made
without departing from the spirit and scope of the present inventions. The following
detailed description is, therefore, not to be taken in a limiting sense, and the scope of the
present invention is defined only by the appended claims.

15 The present invention provides improved methods for performing burn-in testing
of electronic components, such as ICs. By comparing a temperature indication provided
by an on-board thermal sense circuit located on each IC with a gradually decrementing
temperature value, all of the ICs can be characterized or binned according to a desired
thermal parameter, such as junction temperature. Bin split can be improved by adjusting
the burn-in conditions to limit yield loss that results from thermal run-away. Further, a
20 real-time estimate of the burn-in time for each IC is obtained, so that burn-in time can be
adjusted in real-time to maximize burn-in throughput. Various embodiments are
illustrated and described herein, including methods of testing and binning, as well as an
IC having an interface circuit to a burn-in system, an IC burn-in system, and a computer-
readable medium comprising computer instructions for instructing a processor to perform
25 a method of binning a plurality of ICs each having a thermal sense circuit.

30 FIG. 1 illustrates a block diagram of a burn-in system 1 to perform component
burn-in testing and binning, in accordance with one embodiment of the invention. Burn-
in system 1 is merely one example of a burn-in system in which the present invention can
be used. In this example, burn-in system 1 is implemented with a data processing
system.

Burn-in system 1 includes equipment such as a burn-in receptacle or fixture 4 (shown in greater detail in FIG. 3). In one embodiment, fixture 4 contains a plurality of printed circuit boards (PCBs), each of which in turn includes a plurality of ICs undergoing burn-in test; however, in other embodiments, fixture 4 could contain other types of electronic components, examples of which are described elsewhere herein.

5 Burn-in system 1 comprises at least one processor 6. As used herein, "processor" means any type of computational circuit, such as but not limited to a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) 10 microprocessor, an application-specific integrated circuit (ASIC), an artificial intelligence circuit, neural network, or any other type of circuit for performing processing functions, or a combination of such computational circuits.

15 Burn-in system 1 includes a system bus 2 to provide communications links among the various components of burn-in system 1. System bus 2 can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

20 Burn-in system 1 can also include an external memory 10, which in turn can include one or more memory or storage elements, such as a main memory 12 in the form of random access memory (RAM), one or more hard drives 14, and/or one or more drives that handle removable media 16 such as floppy diskettes, compact disks (CDs), tape drives, and the like.

Burn-in system 1 can also include a display device 8 and a keyboard and/or controller 20, which can include a mouse, trackball, voice-recognition device, or any other device that permits a system user to input information into and receive information from burn-in system 1.

25 In operation, processor 6 of burn-in system 1 controls burn-in and/or binning functions under the direction of computer instructions. The computer instructions are stored on one or more computer-readable media within burn-in system 1, including any or all of the memory elements within external memory 10, and/or within memory elements such as high-speed cache (not shown) of processor 6.

30 FIG. 2 illustrates an IC 100 comprising devices to implement burn-in testing and

binning, in accordance with one embodiment of the invention. IC 100 is only one example of an IC that can be tested and/or binned using the present invention.

In the embodiment illustrated in FIG. 2, IC 100 comprises a processor 102, which can be any type of computational circuit such as, but not limited to, those listed earlier.

5 Processor 102 is coupled to bi-directional internal bus 120.

However, the present invention should not be construed as limited to the burn-in and binning of processor ICs, because it can also be applied to any other type of IC, such as memory chips, chipset components, peripheral component interconnect (PCI) devices, bus controllers, high-volume data exchange devices, amplifiers, thyristors, or the like.

10 Any type of IC having an on-board thermal sense circuit can be tested and/or binned using the present invention.

IC 100, in this embodiment, also comprises a memory circuit or memory 104 coupled to internal bus 120. Memory 104 can be of any type or size, provided only that it has sufficient storage space to store a temperature value. In an alternative embodiment, 15 memory 104 can be eliminated from IC 100, and a temperature value is stored in a memory circuit or memory segment of burn-in system 1 (FIG. 1).

IC 100, in this embodiment, also comprises logic circuitry 106 coupled to internal bus 120. Logic circuitry 106 can be of any type, provided only that it can perform a comparison function or match-determining function between a temperature indication 20 generated by thermal sense circuitry 108 and a temperature value stored in memory, either in memory 104 or in burn-in system 1 (e.g. in external memory 10, FIG. 1). In an alternative embodiment, logic circuitry 106 can be eliminated from IC 100, and a match-determining function is performed by processor 6 (FIG. 1) of burn-in system 1.

IC 100 additionally comprises thermal sense circuitry 108 coupled to internal bus 25 120. Thermal sense circuitry 108 can be implemented by any circuit that is capable of generating a temperature parameter or temperature indication. In one embodiment, thermal sense circuitry 108 provides an indication proportional to or indicative of the substrate temperature or junction temperature on IC 100. Thermal sense circuit 108 can be implemented, for example, by a temperature-sensing diode such as a forward-biased 30 diode.

IC 100 also comprises suitable interface circuitry 110 between internal bus 120 and test fixture bus 112, to transmit data, instructions, and/or control signals between IC 100 and burn-in system 1 (FIG. 1).

FIG. 3 is a simplified view of several electronic components 100 mounted on a
5 burn-in test fixture 150, in accordance with one embodiment of the invention. Test board or test fixture 150 comprises a plurality of sockets or connectors (not shown) to which one or more electronic components 100 are coupled. In one embodiment, electronic components 100 are ICs; however, in other embodiments electronic components can be virtually any other type of electronic or electrical device that generates heat in operation.
10 Examples include cellular phones, pagers, computers of all types, electric tools, appliances, entertainment equipment, aerospace and vehicular components, and the like.

Test fixture 150 comprises a bus 112 (FIG. 2) to which electronic components 100 are electrically connected to burn-in system 1 (FIG. 1).

FIG. 4 is a simplified view of test fixtures 150 in a burn-in oven 200, in
15 accordance with one embodiment of the invention. Burn-in test fixtures 150 are situated within an environmentally controlled chamber containing a temperature-altering mechanism, such as a heater and/or a chiller. In one embodiment, the chamber is heated; however, in another embodiment, the chamber could be chilled. Burn-in system 1, operating under the control of a human operator or of computer instructions, thermally
20 stresses the electronic components 100 on test fixtures 150 by, for example, elevating the temperature in burn-in oven 200.

In an embodiment wherein the electronic components 100 being burned-in are ICs, in addition to being heat-stressed they are typically subjected to higher operating voltages. The burn-in voltage varies according to the type of IC and the process used to
25 fabricate it. For example, a burn-in voltage of 2.1 volts is used for one current processor IC product. In addition to increasing the operating voltage, it is desirable to toggle most if not all of the circuit nodes within the ICs during the burn-in period

Thus, while burn-in test fixtures 150 are inside burn-in oven 200, they are functionally connected to burn-in system 1 (FIG. 1) via a network of connectors and
30 wires (not shown) in order to operate the ICs on test fixtures 150 at elevated operating

voltage and to toggle as many circuit nodes as possible on the ICs. Burn-in oven 200 can also include power and clock circuits (not shown) to provide power and clock signals to the ICs undergoing burn-in.

FIGS. 5A and 5B together illustrate a flow diagram of an improved method 500 of testing an IC comprising a plurality of circuits or electronic devices, in accordance with one embodiment of the invention. A first one of the electronic devices provides a temperature indication, and this device can be any suitable thermal sense device, such as thermal sense circuitry 108 (FIG. 2). An optional, second one of the electronic devices stores a temperature value, and this device can be implemented by any suitable memory storage device, such as memory circuit 104 (FIG. 2). If the optional, second memory storage device is not on the IC, the memory storage function can be performed by suitable memory storage within burn-in system 1 (FIG. 1).

In 502, a temperature value is stored for the IC, either in the second electronic device or in a burn-in system coupled to the IC. A temperature value above the highest expected junction temperature of the IC is chosen. For example, in one burn-in embodiment, a temperature value of approximately 110 degrees C is initially stored.

In 504, the IC is thermally stressed by elevating or lowering its ambient temperature. For burning-in ICs, the temperature is raised, e.g. to 60 degrees C.

In 506, the first electronic device (e.g. a temperature sensing diode) provides a temperature indication.

In 508, a determination is made whether the temperature indication matches the stored temperature value. "Match" means having the same value or substantially the same value. If there is a match, the method goes to 510; otherwise, it goes to 512.

In 510, the temperature value is recorded, and the process ends for this IC.

In 512, the temperature value is incremented to a new temperature value, by lowering it one or two degrees (e.g. for a burn-in test), or by raising it one or two degrees (e.g. for a cold test).

In 514, a determination is made whether the temperature indication matches the new stored temperature value. If so, the method goes to 516; otherwise, it returns to 512.

In 516, the temperature value is recorded.

In 518, the process ends for this IC.

FIGS. 6A and 6B together illustrate a flow diagram of an improved method 600 of testing a plurality of electronic components, such as ICs, in accordance with one embodiment of the invention. Electronic components could also be any other type of component besides an IC, examples of which are provided elsewhere in this description.

5 Each electronic component comprises a thermal sense circuit. Each electronic component can also comprise an optional, storage circuit. If the electronic component doesn't have the optional, storage circuit, the memory storage function can be performed

10 by suitable memory storage within burn-in system 1 (FIG. 1). Each electronic component is also identified by a unique identification (ID), which can be of any type but is typically a number.

In 602, a temperature value is stored for each component, either in the component's optional storage circuit or in a burn-in system coupled to the component.

15 In 604, the components are thermally stressed, e.g. by elevating the ambient temperature.

In 606, the thermal sense units each provide a temperature indication for their respective components.

20 In 608, a determination is made whether the temperature indication for each of the plurality of electronic components matches the temperature value. For those components for which this is true, the process goes to 610; otherwise, it goes to 612, for those components for which this is not true.

25 In 610, the temperature value and unique ID are recorded for each electronic component whose temperature indication matched the temperature value in 608. From 610, the process goes to 618.

In 612, the temperature value is changed to a new temperature value (e.g. a lower temperature value for a burn-in operation).

30 In 614, a determination is made whether the temperature indication for each of the plurality of electronic components still being evaluated at this point matches the temperature value. If so, the process goes to 616 for those components for which the

match is true; otherwise, it returns to 612 for those components for which the match is false.

In 616, the temperature value and unique ID are recorded for each electronic component whose temperature indication matched the temperature value in 616. From 5 616, the process goes to 618.

In 618, a determination is made whether all electronic components have had a temperature value recorded for them. If so, the process goes to 620 and ends; otherwise, it returns to 612.

In the present invention, the stimulus pattern for the components being tested 10 during burn-in can be the same for all components under test. It is unnecessary to provide a unique test stimulus pattern to each component undergoing the burn-in test.

FIGS. 7A and 7B together illustrate a flow diagram of a method 700 of instructing a processor to perform a method of binning a plurality of ICs, wherein each 15 IC has a thermal sense circuit and a unique identifier (ID), in accordance with one embodiment of the invention. The processor is an element in a system that includes a temperature-altering mechanism to thermally stress the ICs. In a burn-in system, the temperature-altering mechanism raises the ambient temperature; in a chill-down system, the temperature-altering mechanism lowers the ambient temperature. The system also includes a comparison mechanism that can be implemented in any suitable manner, e.g. 20 using a "compare" program instruction or a hard-wired comparison circuit.

In 702, a temperature value is stored for the ICs undergoing test. For an IC burn-in operation, a temperature value above the highest expected junction temperature of any of the ICs is chosen. For example, in one burn-in embodiment, a temperature value of approximately 110 degrees C is initially stored.

25 In 704, a temperature indication is obtained from the thermal sense circuit of each IC. Each temperature indication is suitably linked with the IC generating it. This can be done, for example, using the IC's ID, and storing an ID/temperature indication pair for each IC under test at this point.

30 In 706, for each IC, the stored temperature value is compared with its own temperature indication.

In 708, a determination is made, for each IC, whether its temperature indication substantially matches the stored temperature value. If so, the process goes to 710; otherwise, it goes to 712.

5 In 710, for each IC for which the match of 708 is true, the temperature value and unique ID are recorded. Also, at this time, using the temperature value recorded for the ICs for which the match of 708 is true, an estimate of the burn-in time can be calculated if desired. This estimate can be further refined as additional ICs are binned in 712 and 714, and in successive iterations of 712 and 714. From 710, the process goes to 718.

10 In 712, the temperature value is changed to a new temperature value (e.g. a lower temperature value for a burn-in operation).

In 714, a determination is made, for each IC, whether its temperature indication substantially matches the new stored temperature value. If so, the process goes to 716; otherwise, it returns to 712.

15 In 716, for each IC for which the match of 714 is true, the temperature value and unique ID are recorded.

In 718, a check is made whether all ICs have had a temperature value and ID recorded for them. If so, the process goes to 720; else, it returns to 712.

In 720, the process ends.

20 The operations described above with respect to the methods illustrated in FIGS. 5, 6A, 6B, 7A, and 7B can be performed in a different order from those described herein.

Determining Junction Temperature T_j for Each Component

The present invention can determine a junction temperature T_j for each IC undergoing a burn-in test. Making use of a temperature indication generated by thermal sense device on-board each IC, the burn-in system initially stores a temperature value above the highest expected junction temperature T_j for the group of ICs undergoing test. By successively comparing the temperature indication output by the thermal sense device of each IC and decrementing the temperature value in successive steps of a degree or two, eventually a match, corresponding to the junction temperature T_j, will be made and recorded for each IC in the group of ICs.

The junction temperature T_j of an IC can be represented by Equation (1) as follows:

Equation (1)
$$T_j = T_a + (\theta_{ja} \times P_d)$$

5

wherein T_j = junction temperature (in degrees C);

T_a = ambient temperature (in degrees C);

θ_{ja} = the junction-to-ambient thermal resistance (in degrees C / watt), which can be in the range of .4 – 2.0 C/watt for some current processor products; and

10 P_d = power dissipation at T_j (in watts), which can be in the range of 10-60 watts for some current processors products.

15 By obtaining a distribution of junction temps for all ICs undergoing burn-in testing, the present invention provides a direct assessment of the burn-in test stability. It also allows an IC manufacturer to substantially remove any thermal margin from burn-in testing by allowing parts having a shorter channel length, and/or parts operating at a higher power or frequency into burn-in testing. It also increases overall bin split, as will now be discussed immediately below.

Increasing Bin Split

20 The present invention provides a relatively high bin split for electronic components undergoing thermal stress testing. “Bin split” is the process of evaluating a group of electronic components, such as ICs, to sort or allocate them into a number of different groups according to some characteristic. The characteristic could be, for example, a performance-related characteristic or an operational-related characteristic, 25 such as standby current I_{SB} . High performance processors generally operate at a higher I_{SB} value (and a correspondingly higher junction temperature T_j) compared with lower performance processors of the same design running at the same clock speed.

In general, the higher the junction temperature T_j , the shorter the burn-in time BITM. However, if the burn-in conditions are set too high, the risk of thermal run-away

increases. By obtaining a T_j for each component, the burn-in conditions can be set to maximize bin split and to limit yield loss that results from thermal run-away.

In this invention, distribution of junction temps between the lowest performance processor and highest performance processor of a batch undergoing burn-in testing can
5 be determined at a relatively fine increment, such as degree-by-degree from 110 degrees C down to 60 degrees C. By obtaining a T_j value for each component, thermal margin is better understood, and transistor channel length L_E can be retargeted (e.g. shortened) to obtain higher frequency bin split.

How the present invention provides for a relatively high bin split will now be
10 discussed.

Each IC has an on-chip thermal sense circuit that provides T_j for the IC. Ambient temperature T_a is maintained constant in the burn-in oven, e.g. at 60 C. Burn-in voltage V_{BI} is maintained constant during burn-in, e.g. $V_{BI} = 2.1$ volts for one current processor product having a normal operating voltage of 1.7 volts.

15 An initial temperature value (e.g. 110 C) is programmed for all ICs, and all ICs are checked to see whether any have a junction temperature indication T_j of 110 C. Any ICs whose T_j is 110 C are identified. For each of these ICs, the ID and the 110 C value are stored.

Next the temperature value is decremented to 109 C, and all ICs are again
20 checked. Any ICs whose T_j is 109 C are identified.

This is continued down to a relatively low temperature, e.g. 60 C, and/or until a T_j value has been logged for all ICs (excepting those that may have failed during burn-in testing). This continuous monitoring of T_j allows the burn-in conditions to be adjusted to minimize yield loss due to thermal run-away, and thus to improve bin split.

25 The ICs are binned according to their T_j values. Those with the highest T_j values are generally capable of highest performance.

Determining Burn-In Time (BITM)

Burn-in testing to screen out infant-mortality failures by testing at elevated
30 voltages and temps is performed for a specified length of time, referred to as the burn-in

time BITM. BITM must be long enough in duration to provide satisfactory statistical and experiential assurance that most, if not all, of the failure-prone electronic components under test will have been identified. However, there is a practical upper limit to BITM duration, which is driven in part by high volume manufacturing costs
5 (including labor costs and energy costs), by production throughput requirements, and by a potential decrease in product reliability in that the stresses applied during burn-in may adversely impact reliability once components are installed in customers' products.

The present invention can achieve significant savings in the burn-in test process by accurately determining the BITM for each component undergoing burn-in testing in
10 the test fixture, as will now be explained.

BITM can be calculated from Equation (2):

Equation (2) $\text{BITM} = A_v * A_T$

15 wherein A_v is a voltage acceleration factor. For one current processor product, A_v is approximately 30.

A_T is a temperature acceleration factor that can vary within ICs of the same design. A_T is derivable from the well-known Arrhenius relationship expressed in
20 Equation (3):

Equation (3) $A_T = \exp [(E_a/k) (1/T_1 - 1/T_2)]$

wherein E_a is an activation energy (in eV), typically in the range of .3-2.0 eV;
k is Bolzmann's constant = 8.617×10^{-5} eV/K;

25 T_1 is the intended use temperature for the IC (in degrees C); and
 T_2 is the burn-in temperature (in degrees C).

A_T is a function of power P_d dissipated from the IC, and it can vary within ICs of the same design. P_d is a function of standby current I_{SB} to the IC, and it can vary within ICs of the same design. I_{SB} is a function of transistor channel length L_E and other process
30 parameters, and it can vary within ICs of the same design.

Using the binning operation performed earlier, A_T can be obtained for each IC, so BITM can be readily calculated in real time for each individual IC undergoing burn-in, using Equation (2) above.

As a result, the BITM can be dynamically varied. For example, BITM can be
5 shortened or lengthened to correspond with the highest calculated BITM for any IC undergoing burn-in.

Alternatively, BITM can be kept relatively constant, but certain test fixtures could be pulled from the burn-in oven early if all of their ICs have completed burn-in, and other test fixtures could be left in the burn-in oven longer, if some of their ICs require a
10 longer than normal burn-in time.

Thus, the burn-in test process can result in significant savings in labor, energy, and production time. It can also result in a significant increase in quality over a burn-in process that uses only a static BITM.

15 Conclusion

The present invention provides improved methods for performing burn-in testing and/or binning of electronic components, such as ICs. By comparing a temperature indication provided by an on-board thermal sense circuit of each IC with a gradually decrementing thermal set-point value, all of the ICs can be characterized or binned
20 according to a desired thermal parameter, such as junction temperature. By employing the burn-in testing concepts of the present invention, it is unnecessary to provide a unique test stimulus pattern to each component under test. The stimulus pattern can be the same for all components undergoing the burn-in test.

A relatively high bin split is obtained, because burn-in conditions can be tuned to
25 minimize thermal run-away loss. In addition, thermal margin based upon T_j can be removed to improve BITM, e.g. by increasing the ambient temperature T_a . Further, a real-time estimate of the burn-in time for each IC is obtained, so that burn-in time can be adjusted to optimize burn-in throughput, and to reduce production costs.

In addition to the above-mentioned methods, an IC having an interface circuit to a
30 burn-in system, an IC burn-in system, and a computer-readable medium comprising

computer instructions for instructing a processor to perform a method of binning a plurality of ICs have been described.

As shown herein, the present invention can be implemented in a number of different embodiments. Other embodiments will be readily apparent to those of ordinary skill in the art. The elements, architecture, functions, and sequence of operations can all be varied to suit particular product and test requirements.

For example, instead of recording the temperature value when a match occurs, the temperature indication could be recorded, because it is either identical to or substantially identical to the temperature value. Also, the components undergoing burn-in testing could be subjected to other environmental accelerators, such as humidity, vibration, thermal cycling, and so forth.

Also, instead of storing a temperature value (e.g. initially a high value), comparing a temperature indication generated by a thermal sense unit on each IC with the temperature value, logging any matches, and then successively decrementing the temperature value until a T_j value has been recorded for all ICs, a slightly different implementation could be used in which a thermal set-point is loaded into each IC. While the ICs are maintained at a constant elevated temperature, the burn-in system checks each IC to determine whether the set-point has been exceeded. If so, it characterizes the component by that set-point; if not, it decrements the set-point and checks again. This process would continue until all ICs have been characterized to a specific set-point. As a result of the method, a junction temperature is obtained for each IC.

The various elements depicted in the drawings are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. The drawings are intended to illustrate various implementations of the invention, which can be understood and appropriately carried out by those of ordinary skill in the art.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiment shown.

This application is intended to cover any adaptations or variations of the present

invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

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